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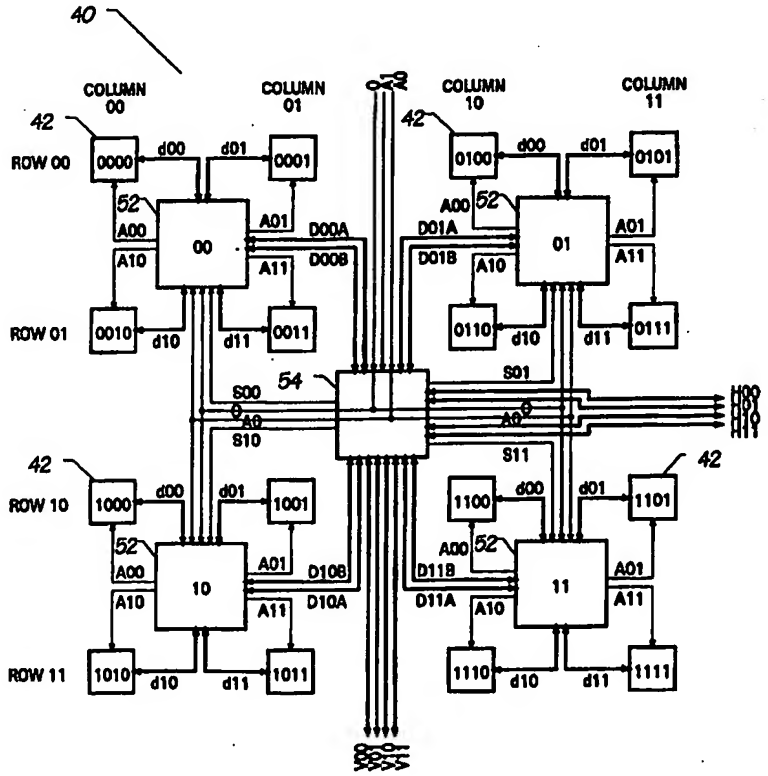
(54) Title: DATA ROUTING DEVICES

(57) Abstract

A data routing device is described which may, for example, be used in field programmable processing arrays, field programmable gate arrays and other reconfigurable logic devices, or which may, for example, be embodied as corner-turning memory. The data routing device comprises at least one connection matrix (40) for routing data in the device, the connection matrix including a plurality of memory cells (42); and means for providing input to and/or output from said memory cells, wherein said means includes a tree structure of input paths to and/or output paths from the memory cell, and wherein each such path of the tree structure includes a set of branching choices (52, 54) along the tree structure.



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TITLE

DATA ROUTING DEVICES

DESCRIPTION

This invention relates to data routing devices, which may, for example, be used in field programmable processing arrays, field programmable gate arrays and other reconfigurable logic devices, or which may, for example, be embodied as corner-turning memory.

The problems with which the present invention (or at least preferred embodiments of it) are concerned are to enable the device to be constructed with a high density of the memory and to permit high-speed operation of the memory.

In accordance with the present invention, there is provided a data routing device, comprising: at least one connection matrix for routing data in the device, the connection matrix including a plurality of memory cells; and means for providing input to and/or output from said memory cells, wherein said means includes a tree structure of input paths to and/or output paths from the memory cells, and wherein each such path of the tree structure includes a set of branching choices along the tree structure.

The use of such a tree structure reduces the amount of wiring which is necessary enabling a high density to be achieved. The device may be constructed so that all of the paths include the same number of branching choices. Also, at any level in the tree structure, the number of branches at any branching choice at that level is preferably equal to the number of branches at the other branching choices at that level. Preferably, the number of branches at each branching choice is two, four or eight. Furthermore, all of the paths are preferably of substantially the same length. These features are particularly advantageous in allowing rapid multiple writes to the memory.

In one embodiment, the connection matrix, or at least one of the connection matrices, includes a plurality of switches; and the memory cells are operable to store data for controlling the switches to define the configuration of the interconnections of that connection matrix. In this case, the connection matrix may be arranged to interconnect a plurality of processing devices or gate arrays.

In another embodiment, the memory cells of the connection matrix, or at least one of the connection matrices, are arranged to receive data in one format, to store the data temporarily, and to output the data in another format. In this case, the memory cells may be arranged as a corner-turning memory, for example for converting data words between nibble-serial format and nibble-parallel format.

The tree structure may provide input paths for addressing the memory cells, with each branching choice being provided by an address decoder which, in response to an input address from a higher level, is operable to sub-address less than all of the address decoders or memory cells at the next lower level. In this case, the address decoders may be operable to sub-address only one or two of the address decoders or memory cells at the next lower level. In one embodiment, at at least one level of the tree structure, the or each address decoder is operable to address a selectable number of the address decoders at the next lower level. This enables multiple simultaneous writes to be made to patterns of the memory cells, which can be particularly advantageous in the case of memory cells which are used for configuring, for example, a field programmable gate or processor array.

Additionally or alternatively, the tree structure may provide input and/or output paths for data to/from the memory cells, with each branching choice being provided by a multiplexer which passes data from the next higher level to less than all of the multiplexers or memory cells at the next lower level and/or which passes to the next higher level data from less than all of the multiplexers or memory cells at the next lower level.

Specific embodiments of the present invention will now be described, purely by way of example, with reference to the accompanying drawings, in which:

Figure 1 shows part of a processor array, illustrating six switching sections and the locations of six arithmetic logic units;

Figure 2 is a diagram of part of the arrangement shown in figure 1 on a larger scale, illustrating one of the switching sections and one of the locations of the arithmetic logic units;

Figure 3 shows part of the processor array shown in figure 1 on a smaller scale, illustrating the locations of the arithmetic logic units and "vertical" busses extending across them;

Figure 4 is similar to figure 3, but illustrating "horizontal" busses extending across the locations of the arithmetic logic units;

Figure 5 shows the interconnections between the busses of figures 2, 3 and 4 at the location of one of the arithmetic logic units;

Figure 6A shows in detail the circuitry of one type of programmable switch in the switching sections, for connecting a pair of 4-bit busses which cross each other;

Figure 6B shows in detail the circuitry of another type of programmable switch in the switching sections, for connecting a pair of 4-bit busses which meet each other end to end;

Figure 6C shows in detail the circuitry of another type of programmable switch in the switching sections, for connecting carry-bit busses;

Figure 7 shows the circuitry of a series of NOR gates which may be used in the

programmable switches of figures 5 and 6;

Figure 8 shows a modification to the circuitry of figure 7;

Figure 9 shows a buffer and register which may be used in each switching section;

Figure 10 is a schematic drawing illustrating how enable signals may be distributed to the programmable switches in the switching sections;

Figure 11 shows in more detail the circuitry of the arrangement shown in figure 10;

Figure 12 shows a "corner-turning" RAM;

Figure 13 illustrates vertical access to a corner-turning RAM;

Figure 14 illustrates horizontal access to a corner-turning RAM;

Figure 15 shows the corner-turning RAM of figure 12 in more detail;

Figure 16 illustrates an example of data paths in the corner-turning RAM of figure 15 when used for vertical access;

Figure 17 illustrates an example of data paths in the corner-turning RAM of figure 15 when used for horizontal access; and

Figure 18 shows a modification to the arrangement described with reference to figures 10 and 11 to allow multiple simultaneous writes to the memory cells.

In the following description, the terms "horizontal", "vertical", "North", "South", "East" and "West" have been used to assist in an understanding of relative directions, but their use is not intended to imply any restriction on the absolute orientation of the

embodiment of the invention.

The processor array which forms the embodiment of the invention is provided in an integrated circuit. At one level, the processor array is formed by a rectangular (and preferably square) array of "tiles" 10, one of which is shown bounded by a thick line in figure 1. Any appropriate number of tiles may be employed, for example in a 16 x 16, 32 x 32 or 64 x 64 array. Each tile 10 is rectangular (and preferably square) and is divided into four circuit areas. Two of the circuit areas 12, which are diagonally opposed in the tile 10, provide the locations for two arithmetic logic units ("ALUs"). The other two circuit areas, which are diagonally opposed in the tile 10, provide the locations for a pair of switching sections 14.

Referring to figures 1 and 2, each ALU has a first pair of 4-bit inputs a, which are directly connected within the ALU, a second pair of 4-bit inputs b, which are also directly connected within the ALU, and four 4-bit outputs f, which are directly connected within the ALU. Each ALU also has an independent pair of 1-bit carry inputs hci, vci, and a pair of 1-bit carry outputs co, which are directly connected within the ALU. The ALU can perform standard operations on the input signals a, b, hci, vci to produce the output signals f, co, such as add, subtract, AND, NAND, OR, NOR, XOR, NXOR and multiplexing and optionally can register the result of the operation. The instructions to the ALUs may be provided from respective 4-bit memory cells whose values can be set via the "H-tree" structure described below, or may be provided on the bus system which will be described below.

At the level shown in figures 1 and 2, each switching section 14 has eight busses extending across it horizontally, and eight busses extending across it vertically, thus forming an 8 x 8 rectangular array of 64 crossing points, which have been numbered in figure 2 with Cartesian co-ordinates. All of the busses have a width of four bits, with the exception of the carry bus vc at X=4 and the carry bus hc at Y=3, which have a width of one bit. At many of the crossing points, a 4-gang programmable switch 16 is provided which can selectively connect the two busses at that crossing point. At some

of the crossing points, a 4-gang programmable switch 18 is provided which can selectively connect two busses which meet end to end at that crossing point, without any connection to the bus at right angles thereto. At the crossing point at (4, 3), a programmable switch 20 (for example as shown in Figure 6C) is provided which can selectively connect the carry busses vc, hc which cross at right angles at that point.

The horizontal busses in the switching section 14 will now be described.

At Y=0, busses h2s are connectable by programmable switches 16 to the vertical busses at X=0, 1, 2, 5, 6. The busses h2s have a length of two tiles and are connectable end to end in every other switching section 14 by a programmable switch 18 at (4, 0).

At Y=1, a bus be extending from an input b of the ALU to the West is connectable by switches 16 to the vertical busses at X=0, 1, 2, 3. Also, a bus fw extending from an output f of the ALU to the East is connectable by switches 16 to the vertical busses at X=5, 6, 7. The ends of the busses be, fw are connectable by a programmable switch 18 at (4, 1).

At Y=2, a bus hregs is connectable by programmable switches 16 to the vertical busses at X=1, 2, 3, 5, 6, 7.

At Y=3, a bus hco extends from the carry output co of the ALU to the West to a programmable switch 20 at (4, 3), which can connect the bus hco (a) to a carry bus hci extending to the carry input hci of the ALU to the East or (b) to a carry bus vci extending to the carry input vci of the ALU to the South.

At Y=4, a bus hregn is connectable by programmable switches 16 to the vertical busses at X=0, 1, 2, 3, 5, 6.

At Y=5, busses h1 are connectable to the vertical busses at X=0, 1, 2, 3, 5, 6, 7. The busses h1 have a length of one tile and are connectable end to end in each switching

section 14 by a programmable switch 18 at (4, 5).

At Y=6, a bus fe extending from an output f of the ALU to the West is connectable by switches 16 to the vertical busses at X=0, 1, 2, 3. Also, a bus aw extending from an input a of the ALU to the East is connectable by switches 16 to the vertical busses at X=5, 6, 7. The ends of the busses fe, aw are connectable by a programmable switch 18 at (4, 6).

At Y=7, busses h2n are connectable by programmable switches 16 to the vertical busses at X=1, 2, 3, 6, 7. The busses h2n have a length of two tiles and are connectable end to end in every other switching section 14 by a programmable switch 18 at (4, 7), staggered with respect to the programmable switches 18 connecting the busses h2s at (4, 0).

The vertical busses in the switching section 14 will now be described.

At X=0, busses v2w are connectable by programmable switches 16 to the horizontal busses at Y=0, 1, 4, 5, 6. The busses v2w have a length of two tiles and are connectable end to end in every other switching section 14 by a programmable switch 18 at (0, 3).

At X=1, a bus fn extending from an output f of the ALU to the South is connectable by programmable switches 16 to the horizontal busses at Y=0, 1, 2. Also, a bus bs extending from an input b of the ALU to the North is connectable by switches 16 to the horizontal busses at Y=4, 5, 6, 7. The ends of the busses fn, bs are connectable by a programmable switch 18 at (1, 3).

At X=2, busses v1 are connectable to the horizontal busses at Y=0, 1, 2, 4, 5, 6, 7. The busses v1 have a length of one tile and are connectable end to end in each switching section 14 by a programmable switch 18 at (2, 3).

At X=3, a bus vregw is connectable by programmable switches 16 to the horizontal busses at Y=1, 2, 4, 5, 6, 7.

At X=4, a bus vco extends from the carry output co of the ALU to the North to the programmable switch 20 at (4, 3), which can connect the bus vco (a) to the carry bus hci extending to the carry input hci of the ALU to the East or (b) to the carry bus vci extending to the carry input vci of the ALU to the South.

At X=5, a bus vrege is connectable by programmable switches 16 to the horizontal busses at Y=0, 1, 2, 4, 5, 6.

At X=6, a bus an extending from an input a of the ALU to the South is connectable by switches 16 to the horizontal busses at Y=0, 1, 2. Also, a bus fs extending from an output f of the ALU to the North is connectable by programmable switches 16 to the horizontal busses at Y=4, 5, 6, 7. The ends of the busses an, fs are connectable by a programmable switch 18 at (6, 3).

At X=7, busses v2e are connectable by programmable switches 16 to the horizontal busses at Y=1, 2, 5, 6, 7. The busses v2e have a length of two tiles and are connectable end to end in every other switching section 14 by a programmable switch 18 at (7, 3) staggered with respect to the programmable switches 18 connecting the busses v2w at (0, 3).

As shown in figure 2, the busses bs, vco, fs are connected to input b, output co and output f, respectively, of the ALU to the North of the switching section 14. Also, the busses fe, hco, be are connected to the output f, output co and input b of the ALU, respectively, to the West of the switching section 14. Furthermore, the busses aw, hci, fw are connected to the input a, input ci and output f, respectively, of the ALU to the East of the switching section 14. Moreover, the busses fn, vci, an are connected to the output f, input ci and input a, respectively, of the ALU to the south of the switching section 14.

In addition to these connections, the busses vregw, vrege are connected via respective programmable switches 18 to 4-bit connection points vtsw, vtse, respectively, (shown by crosses in Figure 2) in the area 12 of the ALU to the North of the switching section 14. Also, the busses hregs, hregn are connected via respective programmable switches 18 to 4-bit connection points htse, htne, respectively, in the area 12 of the ALU to the West of the switching section 14. Furthermore, the busses hregs, hregn are connected via respective programmable switches 18 to 4-bit connection points htsw, htnw, respectively, in the area 12 of the ALU to the East of the switching section 14. Moreover, the busses vregw, vrege are connected via respective programmable switches 18 to 4-bit connection points vtnw, vtne, respectively, in the area 12 of the ALU to the south of the switching section 14. These connection points vtnw, vtne, htne, htse, vtse, vtsw, htsw, htnw will be described below in further detail with reference to figures 3 to 5.

Also, as shown in figure 2, the busses hregn, vrege, hregs, vregw have respective 4-bit connection points 22 (shown by small squares in figure 2) which will be described below in further detail with reference to figure 9.

Figure 3 shows one level of interconnections between the locations of the arithmetic logic units, which are illustrated by squares with rounded corners. A group of four 4-bit busses v8, v4w, v4e, v16 extend vertically across each column of ALU locations 12. The leftmost bus v8 in each group is in segments, each having a length generally of eight tiles. The leftmost but one bus v4w in each group is in segments, each having a length generally of four tiles. The rightmost but one bus v4e in each group is in segments, again each having a length generally of four tiles, but offset by two tiles from the leftmost but one bus v4w. The rightmost bus v16 in each group is in segments, each having a length generally of sixteen tiles. At the top edge of the array, which is at the top of figure 4, and at the bottom edge the lengths of the segments may be slightly greater than or shorter than specified above.

Referring to figures 3 and 5, where each group of four busses v8, v4w, v4e, v16 crosses

each ALU location 12, four 4-bit tap connections are made at the connection points htnw, htsw, htse, htne. The ends of the bus segments take priority in being so connected over a connection to a bus segment which crosses the ALU location.

Similarly, as shown in figures 4 and 5, a group of four 4-bit busses h8, h4n, h4s, h16 extend horizontally across each row of ALU locations 12. The uppermost bus h8 in each group is in segments, each having a length generally of eight tiles. The uppermost but one bus h4n in each group is in segments, each having a length generally of four tiles. The lowermost but one bus h4s in each group is in segments, again each having a length generally of four tiles, but offset by two tiles from the uppermost but one bus h4n. The lowermost bus h16 in each group is in segments, each having a length generally of sixteen tiles. At the left hand edge of the array, which is at the left of figure 4, and at the right hand edge the lengths of the segments may be slightly greater than or shorter than specified above. Where each group of busses h8, h4n, h4s, h16 crosses each ALU location 12, a further four 4-bit tap connections are made at the connection points vtnw, vtsw, vtse, vtne. The ends of the bus segments take priority in being so connected over a connection to a bus segment which crosses the ALU location.

As shown in figure 5, the connection points htnw, htsw, htne, htse are connected via programmable switches to the busses hregn, hregs of the switching sections to the West and the East of the ALU location. Also, the connection points vtnw, vtne, vtsw, vtse are connected via programmable switches to the busses vregw, vrege of the switching sections to the North and the South of the ALU location.

The programmable connections 16 between pairs of 4-bit busses which cross at right angles will now be described with reference to figure 6A. The conductors of the horizontal busses are denoted as x0, x1, x2, x3, and the conductors of the vertical busses are denoted as y0, y1, y2, y3. Between each pair of conductors of the same bit significance, a respective transistor 160, 161, 162, 163 is provided. The gates of the transistors 160, 161, 162, 163 are connected in common to the output of a NOR gate 16g, which receives as its two inputs an inverted ENABLE signal from a single bit

memory cell, which may be shared by a group of the switches, and the inverted content of a single bit memory cell 24. Accordingly, only when the ENABLE signal is high and the content of the memory cell 24 is high, the conductors x0, x1, x2, x3 are connected by the transistors 160, 161, 162, 163, respectively, to the conductors y0, y1, y2, y3, respectively.

The programmable connections 18 between pairs of 4-bit busses which meet each other end to end in line will now be described with reference to figure 6B. The conductors of one bus are denoted as x10, x11, x12, x13, and the conductors of the other bus are denoted as x20, x21, x22, x23. Between each pair of conductors of the same bit significance, a respective transistor 180, 181, 182, 183 is provided. The gates of the transistors 180, 181, 182, 183 are connected in common to the output of a NOR gate 18g, which receives as its two inputs an inverted ENABLE signal from a single bit memory cell, which may be shared by a group of the switches, and the inverted content of a single bit memory cell 24. Accordingly, only when the ENABLE signal is high and the content of the memory cell 24 is high, the conductors x10, x11, x12, x13 are connected by the transistors 180, 181, 182, 183, respectively, to the conductors x20, x21, x22, x23, respectively.

The programmable connections 20 between the carry conductors hco,vco,hci,vci will now be described with reference to figure 6C. The horizontal carry output conductor hco is connected to the horizontal carry input conductor hci and the vertical carry input conductor vci via transistors 20hh, 20hv, respectively. Furthermore, the vertical carry output conductor vco is connected to the vertical carry input conductor vci and the horizontal carry input conductor hci via transistors 20vv, 20vh, respectively. The gates of the transistors 20hh, 20vv are connected in common to the output of an inverter 20i, and the gates of the transistors 20hv, 20vh and the input to the inverter 20i are connected to the output of a NOR gate 20g. The NOR gate 20g receives as its two inputs an inverted ENABLE signal from a single bit memory cell, which may be shared by a group of the switches, and the inverted content of a single bit memory cell 24. Accordingly, when the ENABLE signal is high, the conductors hco, vco are connected

to the conductors hci, vci, respectively, or to the conductors vci, hci, respectively, in dependence upon the content of the memory cell 24.

It will be noted that each of the switchable connections 16, 18, 20 described with reference to figures 6A to 6C includes a NOR gate 16g, 18g, 20g. As shown in figure 7, a NOR gate 16g is typically formed by four transistors 16g1, 16g2, 16g3, 16g4, two 16g1, 16g3 of which are responsive to the inverted ENABLE signal, and two 16g2, 16g4 of which are responsive to the inverted content of the memory cell 24. In the embodiment of the invention, it is desirable that a group of the switchable collections 16, 18, 20 may be disabled in common, without any need for only part of such a group to be disabled. Such a group might consist of all of the switchable connections in one switching section 14, all of the switchable connections in the two switching sections 14 in a particular tile, or all of the switchable connections in a larger area of the array. In this case, the transistor 16g1 may be made common to all of the switchable connections 16, 18, 20 in the group, as shown in figure 8. This enables a 25% less one saving in the number of transistors required for the gates, but does require a further conductor linking the gate, as shown in figure 8.

As mentioned above with reference to figures 1 and 2, at each switching section 14, the busses hregn, hregs, vregw, vrege are connected by respective 4-bit connections 22 to a register or buffer circuit, and this circuit will now be described in more detail with reference to figure 9. The four connections 22 are each connected to respective inputs of a multiplexer 26. The multiplexer 26 selects one of the inputs as an output, which is supplied to a register or buffer 28. The output of the register or buffer 28 is supplied to four tri-state buffers 30s, 30w, 30n, 30e, which are connected back to the connections 22 to the busses hregs, vregw, hregn, vrege, respectively. In the case where a buffer 28 is used, the 4-bit signal on a selected one of the busses hregs, vregw, hregn, vrege is amplified and supplied to another selected one of the busses hregs, vregw, hregn, vrege. In the case where a register 28 is used, the 4-bit signal on a selected one of the busses hregs, vregw, hregn, vrege is amplified and supplied to any selected one of the busses hregs, vregw, hregn, vrege after the next active clock edge.

It will be appreciated that the arrangement described above provides great flexibility in the routing of signals around and across the array. With appropriate setting of the switches 16, 18, 20 using the memory cells 24 and with appropriate setting of the multiplexers 26 and registers or buffers 28, signals can been sent over large distances, primarily using the busses v16, h16, v8, h8, v4e, v4w, h4n, h4s from the edge of the array to a particular ALU, between ALUs, and from a particular ALU to the edge of the array. These busses can be joined together in line, or at right angles, by the switching sections 14, with amplification by the registers or buffers 28 in order to reduce propagation delays, and with pipeline stages introduced by the registers 28. Also, these busses can be tapped part way along their lengths, so that the siting of the ALUs to perform a particular processing operation is not completely dictated by the lengths of the busses, and so that signals can be distributed to more than one ALU. Furthermore, the shorter length busses described with reference to figures 1 and 2 can be used to route signals between the switching sections 14 and the ALUs, and to send signals primarily over shorter distances, for example from one ALU to an adjacent ALU in the same row or column, or diagonally adjacent, even though the busses extend horizontally or vertically. Again, the registers or buffers 28 can be used to amplify the signals or introduce programmable delays into them.

In the arrangement described above, the memory cells 24 are distributed across the array to the same extent as the switching sections 14 and the ALU locations 12. Each memory cell 24 is disposed adjacent the switch or switches, multiplexer, register or buffer which it controls. This enables a high circuit density be achieved.

A description will now be made of the manner in which data is written to or read from the memory cells 24, the way in which the ENABLE signals for the programmable switches 16, 18, 20 are written to their memory cells, the way in which instructions, and possibly constants, are distributed to the ALUs, and the way in which other control signals, such as a clock signal, are transmitted across the array. For all of these functions, an "H-tree" structure may be employed, as shown in figure 10. Referring to Figures 10 and 11, in order to distribute an ENABLE signal to any of 64 locations in

the example shown, the ENABLE signal 30a and a 6-bit address 32a for it are supplied to a decoder 34a. The decoder 34a determines which of the four branches from it leads to the address and supplies an ENABLE signal 30b to a further decoder 34b in that branch, together with a 4-bit address 32b to the decoders 34b in all four branches. The decoder 34b receiving the ENABLE signal 30b determines which of the four branches from it leads to the required address and supplies an ENABLE signal 30c to a further decoder 34c in that branch, together with a 4-bit address 32c to the decoders 34c in all four branches. The decoder 34c receiving the ENABLE signal 30c then supplies the ENABLE signal 34d to the required address where it can be stored in a single bit memory cell. An advantage of the H-tree structure is that the lengths of the signal paths to all of the destinations are approximately equal, which is particularly advantageous in the case of the clock signal.

A great advantage of the arrangement described above is that groups of the memory cells 24 in for example one switching section 14, or in the two switching sections in one tile, or in the switching sections in a sub-array of the tiles may be disabled en bloc by the inverted ENABLE signals so that the contents of those memory cells do not affect the associated switches. It is then possible for those memory cells 24 to be used as "user" memory by an application, rather than being used for configuring the wiring of the array.

The embodiment of the invention has been described merely by way of example, and many modifications and developments may be made in keeping with the present invention. For example, the embodiment employs ALUs as the processing units, but other processing units may additionally or alternatively be used, for example look-up tables, programmable logic arrays and/or self-contained CPUs which are able to fetch their own instructions.

Furthermore, the embodiment has been described as if the whole array is covered by ALUs and switching sections. However, other types of section may be included in the array. For example, a sub-array might be composed of a 4 x 4 arrangement of tiles of

ALUs and switching sections as described above, and the array might be composed of such sub-arrays and memory in a 4 x 4 array, or such sub-arrays and RISC CPUs in a 4 x 4 array.

In the embodiment described above, each ALU location is square, and each switching section is square and of the same size as the ALU locations, but it should be noted that the controllable switches 18 in the register busses vregw, vrege, hregn, hregs encroach into the square outline of the ALU locations. The ALU locations need not be of the same size as the switching sections, and in particular may be smaller, thus permitting one or more busses to pass horizontally or vertically directly from one switching section 14 to a diagonally adjacent switching section 14, for example running between the busses h2s, h2n or between the busses v2e, v2w.

In the embodiment described above, each ALU has two independent carry inputs vci, hci and a connected pair of carry outputs co. If required, the ALUs may be arranged to deal with two types of carry: a fast carry between adjacent ALUs which may be of particular use for multi-bit adding operations; and a slow carry which can be routed more flexibly and may be of particular use for digital serial arithmetic. The fast carry might be arranged in a similar manner to that described above with reference to the drawings, whereas the slow carry might employ programmable switches in the switching sections 14 between the carry conductor and particular bits of the 4-bit busses.

In the embodiment described above, particular bit widths, sizes of switching section and sizes of array have been mentioned, but it should be noted that all of these values may be changed as appropriate. Also, the programmable switches 16, 18, 20 have been described as being disposed at particular locations in each switching section 14, but other locations may be used as required and desired.

In the embodiment described above, the array is two-dimensional, but the principles of the invention are also applicable to three-dimensional arrays, for example by providing a stack of the arrays described above, with the switching sections in adjacent layers

staggered with respect to each other. The stack might include just two layers, but preferably at least three layers, and the number of layers is preferably a power of two.

In the embodiment described above, the memory cells 24 can be isolated by the gates 16g, 18g, 20g from the switches which they control so that the memory cells can be used for other purposes, that is put in the "user plane". The ENABLE signal memory cells, however, cannot be transferred to the user plane. In an alternative embodiment, the switches in a particular switching section 14 may be disconnectable from the remainder of the array by further switches in the busses at the boundary of that switching section 14, with the further switches being controlled by a further memory cell which cannot be transferred to the user plane.

A further embodiment of the present invention will now be described with reference to figures 12 to 17. This embodiment is applied to a corner-turning RAM 40, the principle of operation of which is shown in figure 12. As shown, the RAM 40 comprises a 4x4 array of memory cells 42, each of which can store four bits (ie a nibble) of data. The RAM 40 has two ports 44, 46, one 44 of which operates with data in nibble-parallel format, reading or writing rows of data, each constituting a word, into the RAM 40. The other port operates with data in nibble-serial format, reading or writing corresponding columns of data into the RAM 40, each column containing corresponding nibbles from multiple words of data.

The corner-turning RAM may be used in combination with the first embodiment of the invention. For example, in order to perform operations with 16-bit precision on 16-bit operands, with the first embodiment four of the ALUs may be used. However, in order to conserve ALU use, a single ALU may be used handling the operands in nibble-serial format. A corner-turning RAM 40 may therefore be used firstly to convert the operands from nibble-parallel format to nibble-serial format and then to convert the result from nibble-serial format back to nibble-parallel format. The corner-turning RAM 40 may, of course, also be used independently of the first embodiment of the invention.

Although figure 12 shows the corner-turning RAM as a square array, this is not necessary. The width of the array is determined by the width of the nibble-parallel port, and the height is determined by the number of parallel worlds to be extracted from the nibble-serial port. These are two independent design parameters. Furthermore, in principle, neither the width nor the height need be a power of two nibbles, but power-of-two dimensions can conveniently be chosen to simplify the control of the RAM 40. Because the arrangement described below works best with power-of-two RAM dimensions, this will be described, but the vertical and horizontal dimensions may be different.

For correct operation, the whole RAM 40 needs to be written in one orientation before being read in the other orientation. For example, if a column is read before all four rows have been written, the nibbles from the unwritten rows will contain invalid data. Also, the whole RAM contents need to be read in the reading orientation before new data is written into the same address space in the RAM 40 from the writing side. For these reasons, the corner-turning RAM may be used in pairs, to allow double-buffering.

In this further embodiment of the invention, the corner-turning RAM 40 is implemented in a hierarchical fashion, with each level of hierarchy including a factor of two increase in memory size in either or both directions. Figures 13 and 14 show a single level of hierarchy that includes a factor of two size increase in both directions, making a factor of four overall.

When accessing the memory vertically, as shown in figure 13, one address bit is used to determine which row of the two lower level rows of blocks 42 is accessed, either low address or high address. The two accessed blocks are accessed in parallel in this case using the data bus V0 for the four bits of the low nibble and the data bus V1 for the four bits of the high nibble. By contrast, figure 14 illustrates access to the hierarchical corner-turning RAM when made horizontally, rather than vertically. In this case, one address bit is used to determine which column of the two lower level columns of blocks 42 is accessed, the low address or high address. The two accessed blocks are accessed in

parallel using the data bus H0 for the four bits of the lower nibble and the data bus H1 for the four bits of the high nibble. It will be noted from figures 13 and 14 that, with either orientation of access, the top-left block 42 has the low address and the low nibble, and the bottom-right block 42 has the high address and the high nibble. However, the top-right block 42 changes between low-address/high-nibble during vertical access and high-address/low-nibble during horizontal access, and the bottom left block 42 changes between high-address/low-nibble for vertical access and low-address/high-nibble for horizontal access. The address decoding and data multiplexing at this level of the hierarchical RAM 40 needs to be controllable according to the access orientation to allow the RAM to be used as a corner-turning RAM.

In a larger hierarchical corner-turning RAM, the address decoding and data multiplexing at each level of the hierarchy is controlled according to the access orientation, as described above.

Figure 15 illustrates a corner-turning RAM 40 having two levels of hierarchy in each direction, thus providing a 16-fold increase in memory size, and which employs an "H-tree" structure for both the address paths and the data paths. In figure 15, the 4-bit memory cells 42 have been marked with 4-bit labels 0000 to 1111; the columns of the memory cells 42 have been marked with two-bit addresses 00 to 11; and the rows of the memory cells 42 have been marked with two-bit addresses 00 to 11. The four 2x2 groups of the memory cells 42 each have a respective lower-level address decoder and data multiplexer 52 labelled 00 to 11, and there is a central higher-level address decoder and data multiplexer 54.

The addressing operation of the RAM 40 of figure 15 will now be described. The higher-level decoder/multiplexer 54 receives two signals A0, A1 giving the address of the row or the column of the memory cells 42 to be accessed, together with a signal O indicating whether vertical (logic level "0") or horizontal (logic level "1") access is required. The signal A0 is passed directly to the lower-level decoder/multiplexers 52. The signal A1 is used by the higher-level decoder 54. The signal O is both used by the

higher-level decoder/multiplexer 54 and is also passed on to the lower-level decoder/multiplexers 52. The higher-level decoder/multiplexer 54 produces four select signals S00 to S11, which are supplied to the respective lower-level decoder/multiplexers 52(00) to 52(11) and are generated according to the following:

S00 = not(A1)

S01 = (not(A1) and not(O)) or (A1 and O)

S10 = (not(A1) and O) or (A1 and not(O))

S11 = A1

The lower-level decoder/multiplexers 52 each produce four address signals A00 to A11 which are supplied to the respective memory cells 42 serviced by that decoder/multiplexer 52 and are generated according to the following:

A00 = Sxx and not(A0)

A01 = Sxx and ((not(A0) and not(O)) or (A0 and O))

A11 = Sxx and ((not(A0) and O) or (A0 and not(O)))

A11 = Sxx and A0

where Sxx denotes the respective select signal S00 to S11 received by that lower-level decoder/multiplexer 52.

Accordingly, it will be appreciated that, with vertical access (O=0), a row of the memory cells 42 is addressed as designated by the address signals A0, A1. By contrast, with horizontal access (O=1), a column of the memory cells 42 is addressed as designated by the address signals A0, A1.

The data paths of the RAM 40 of figure 15 will now be described. The input/output data path for vertical access is shown as four 4-bit busses V00 to V11 connecting to the higher-level decoder/multiplexer 54, and the input/output data path for horizontal access is shown as four 4-bit busses H00 to H11 also connected to the higher-level decoder/multiplexer 54. Each of the lower-level decoder/multiplexers 52(xx) is connected to the higher-level decoder/multiplexer 54 by two 4-bit data busses DxxA, DxxB. Also, each of the lower-level decoder/multiplexers 52 is connected to each of its

memory cells 42 by respective 4-bit data busses d00 to d11. The logical relations by which the lower-level decoder/multiplexers 52 connect the data busses d00 to d11 to the data busses DxxA, DxxB are similar to those employed by the decoder/multiplexers 52 for addressing the memory cells 42. Furthermore, the logical relations by which the higher-level decoder/multiplexers 54 connect the data busses DxxA, DxxB to the vertical and horizontal data busses V00 to V11, H00 to H11 are similar to those employed by the decoder/multiplexer 54 for addressing selecting the lower-level decoder/multiplexers 52.

For example, as shown in figure 16, when the address inputs are O=0, A1=1 and A0=0, denoting that the memory cells 42 in row 10 should be connected to the vertical input/output busses V00-V11, the lower-level decoder/multiplexer 52(10) connects its memory cell data busses d00, d01 to the data busses D10A, D10B, respectively, and the higher-level decoder/multiplexer 54 connects the data busses D10A, D10B to the vertical input/output busses V00, V01, respectively. Also, the lower-level decoder/multiplexer 52(11) connects its memory cell data busses d00, d01 to the data busses D11B, D11A, respectively, and the higher-level decoder/multiplexer 54 connects the data busses D11B, D11A to the vertical input/output busses V10, V11, respectively. Accordingly, the memory cells 42 in row 10 are connected to the vertical input/output data busses V00-V11 in the correct order.

Figure 17 shows another example where the address inputs are O=1, A1=0 and A0=1, denoting that the memory cells 42 in row 01 should be connected to the horizontal input/output busses H00-H11. In this case, the lower-level decoder/multiplexer 52(00) connects its memory cell data busses d01, d11 to the data busses D00A, D00B, respectively, and the higher-level decoder/multiplexers 54 connects the data busses D00A, D00B to the horizontal input/output busses H00, H01, respectively. Furthermore, the lower-level decoder/multiplexer 52(10) connects its memory cell data busses d01, d11 to the data busses D10B, D10A, respectively, and the higher-level decoder/multiplexer 54 connects the data busses D10B, D10A to the horizontal input/output busses H10, H11, respectively. Accordingly, the memory cells 42 in

column 01 are connected to the horizontal input/output data busses H00-H11 in the correct order.

It will be appreciated that many modifications and developments may be made to the second embodiment of the invention. For example, as mentioned above, the array of memory cells need not be square, and neither the height nor the width of the array need be a power of two.

Also, although the H-tree structure has been employed both for the addressing paths and the data paths, it may be employed for only one of these.

Furthermore, although separate horizontal and vertical busses H00-H11, V00-V11 have been described above, these busses may alternatively share the same conductors.

Figure 18 shows a modification to the arrangement of figures 10 and 11 for writing data to a hierarchical RAM for configuring a field programmable gate array, field programmable processor array or the like. Configuring large arrays of this type requires a large amount of data, and loading the data can occupy the memory and bus bandwidths for extended periods of time. A technique which reduces the amount of data to be loaded into the array can reduce the memory storage requirements, the bus bandwidth requirements and the delay in loading a new configuration.

An array configuration for a regular computation is regular itself. In other words, multiple identical pieces of circuitry can be laid out so that they are all identical, and so that they "tile" neatly. This regularity can be exploited so that only one copy of be configuration data for the repeated circuitry needs to be loaded, and the single copy can be distributed to the multiple locations where copies of the circuitry are to be placed.

In figure 18, a higher-level address decoder 54 receives a 4-bit address A00,A01,A10,A11. The two more-significant bits A10,A11 are used to produce signals S00,S01,S10,S11, each of which is supplied to a respective one of four lower-level

address decoders 52 labelled 00,01,10,11, so that in normal operation only one of the four decoders 52 is selected. The two less-significant bits A00,A01 are simply passed to the four lower-level decoders 52. Each of the lower-level decoders 52, if selected by its respective select signal Sxx, addresses a respective one of its four memory cells 42 in dependence upon the two-bit address A00,A01, and data D which is provided to all of the lower-level decoders 52 is written to the addressed memory cell 42. Accordingly, the data D is written only one of the sixteen memory cells 42. Thus, in this mode of operation, the decoding operation performed by the higher-level decoder 54 is defined by the following:

S00 = not(A10) and not(A11);

S01 = A10 and not(A11);

S10 = not(A10) and A11;

S11 = A10 and A11.

For each of the more-significant address bits A10,A11 the higher-level decoder 54 also receives a respective wild-card bit W10,W11. The higher-level decoder 54 is arranged so that, if either of the wild-card bits W10,W11 is set, the respective address bit A10,A11 is wild-carded. Thus, the decoding operation performed by the higher-level decoder 54 becomes as follows:

S00 = {not(A10) or W10} and {not(A11) or W11};

S01 = {A10 or W10} and {not(A11) or W11};

S10 = {not(A10) or W10} and {A11 or W11};

S11 = {A10 or W10} and {A11 or W11}.

Accordingly, if the wild-card bit W10 is set, two of the memory cells 42, in the left half and right half, respectively, of the array, will be addressed. If the wild-card bit W11 is set, two of the memory cells 42 in the upper half and lower half, respectively, of the array, will be addressed. Furthermore, if both of the wild-card bits W10,W11 are set four of the memory cells 42 to the top-left, top-right, bottom-left and bottom-right of the array will be addressed. Therefore, it is possible to make multiple simultaneous writes to the array in a single cycle.

The arrangement described with respect to figure 18 may be modified. For example, the wild-card bits may be associated with the address bits A00,A01 for the lower level decoders 52, so that multiple writes may be made to the two memory cells 42 to the left, to the right, above or below the addressed lower-level decoder 52, or to all four of the memory cells 42 associated with the addressed lower-level decoder 52. Furthermore, such wild-card bits may be associated with all of the address bits A00,A01,A10,A11 or with only some of them.

The technique of multiple writes has been described with reference to a hierarchical memory having only two levels of decoder, and it will be appreciated that the technique may be used with hierarchical memory having more than two levels, and may be applied to one, some or all of those levels.

In the arrangement described above with reference to figure 18, the width of the address bus is increased by one for each address bit which is to have the capability of being wild-carded. Nevertheless, the wild-card information can be modified on a cycle-by-cycle basis without a performance penalty. In a modified arrangement, the wild-card inflation is stored adjacent each decoder in a memory cell for each wild-card bit and is pre-loaded into the wild-card memory cells. This reduces the cost of wiring, but requires additional storage paths and operating cycles for changing the wild-carding information.

Many other modifications and developments may also be made. For example, in arrangements like that of figure 18, the higher or highest level decoder 54 produces its four output signals S00,S01,S10,S11 from four input signals A10,W10,A11,W11. Alternatively, the four signals S00,S01,S10,S11 could be directly fed into the arrangement for the same wiring cost and obviating the need for the higher or highest level decoder.

CLAIMS

1. A data routing device, comprising:

at least one connection matrix (14;40) for routing data in the device, the connection matrix including a plurality of memory cells (24;42); and

means for providing input to and/or output from said memory cells, wherein said means includes a tree structure of input paths to and/or output paths from the memory cells, and wherein each such path of the tree structure includes a set of branching choices (34;52,54) along the tree structure.

2. A device as claimed in claim 1, wherein all of the paths include the same number of branching choices.

3. A device as claimed in claim 1 or 2, wherein, at any level in the tree structure, the number of branches at any branching choice at that level is equal to the number of branches at the other branching choices at that level.

4. A device as claimed in any preceding claim, wherein the number of branches at each branching choice is two, four or eight.

5. A device as claimed in any preceding claim, wherein all of the paths are of substantially the same length.

6. A device as claimed in any preceding claim, wherein:

the connection matrix, or at least one of the connection matrices, includes a plurality of switches (16,18,20); and

the memory cells (24) are operable to store data for controlling the switches to define the configuration of the interconnections of that connection matrix.

7. A device as claimed in claim 6, wherein the connection matrix is arranged to interconnect a plurality of processing devices (12) or gate arrays.

8. A device as claimed in any preceding claim, wherein the memory cells (42) of the connection matrix, or at least one of the connection matrices, are arranged to receive data in one format, to store the data temporarily, and to output the data in another format.

9. A device as claimed in claim 8, wherein the memory cells are arranged as a corner-turning memory (40).

10. A device as claimed in any preceding claim, wherein the tree structure provides input paths (32;O,A0,A1,S00-S11) for addressing the memory cells, each branching choice being provided by an address decoder (34;52,54) which, in response to an input address from a higher level, is operable to sub-address less than all of the address decoders or memory cells at the next lower level.

11. A device as claimed in claim 10, wherein at least one of the address decoders (34) is operable to sub-address one of the address decoders or memory cells at the next lower level.

12. A device as claimed in claim 10, wherein at least one of the address decoders (52,54) is operable to sub-address two of the address decoders or memory cells at the next lower level.

13. A device as claimed in any of claims 10 to 12, wherein, at at least one level of the tree structure, the or each address decoder is operable to address a selectable number of the address decoders at the next lower level.

14. A device as claimed in any preceding claim, wherein the tree structure provides input and/or output paths (H00-H11,V00-V11,D00A-D11A,D00B-D11B,d00-d11) for data to/from the memory cells, each branching choice being provided by a multiplexer (52,54) which passes data from the next higher level to less than all of the multiplexers or memory cells at the next lower level and/or which passes to the next higher level data

from less than all of the multiplexers or memory cells at the next lower level.

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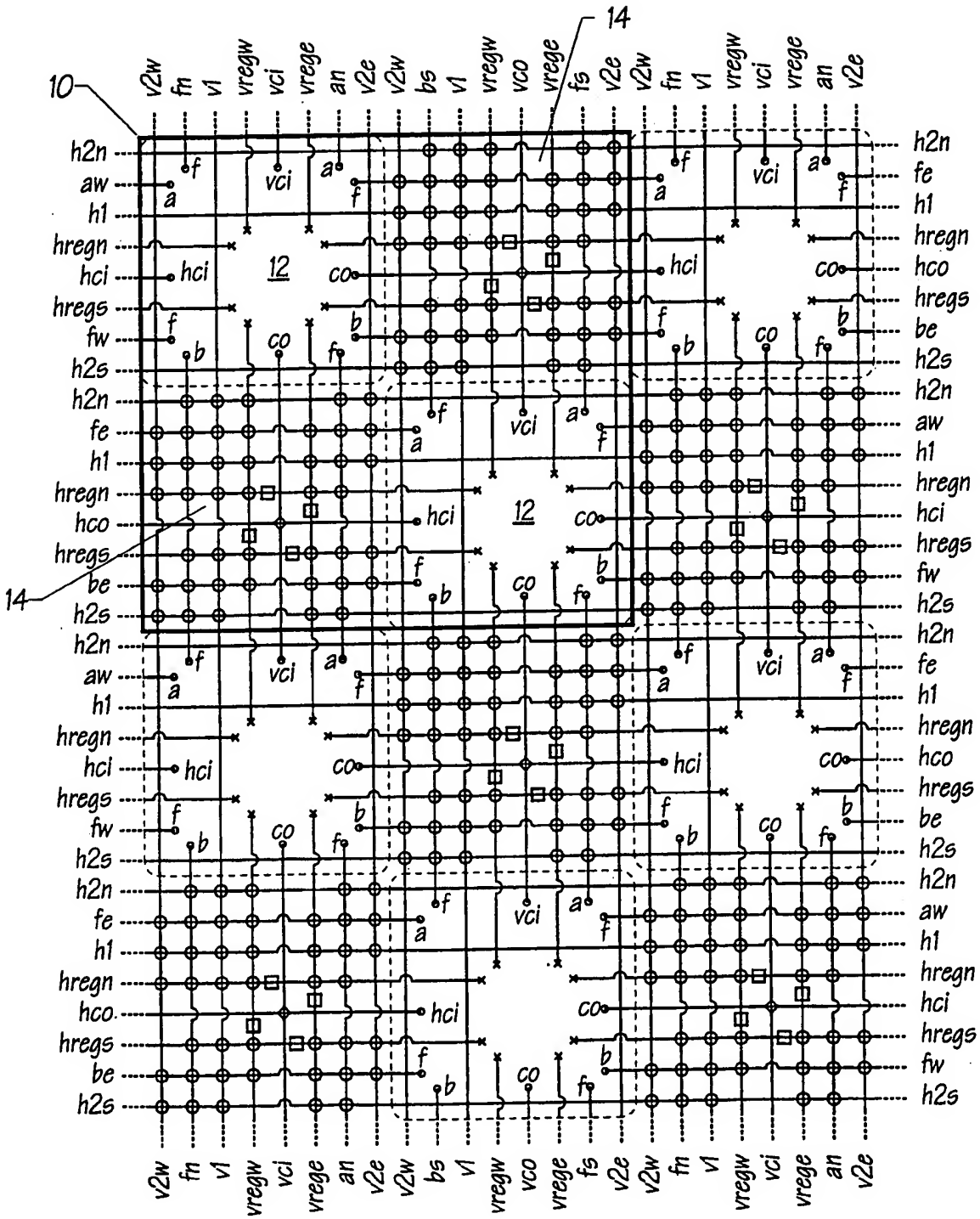
10
14
12
12
v2w
fn
v1
vregw
vci
vrege
an
v2e
bs
vco
fs
h2n
aw
h1
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be
a
b
f
co
hci
vci

FIG. 1

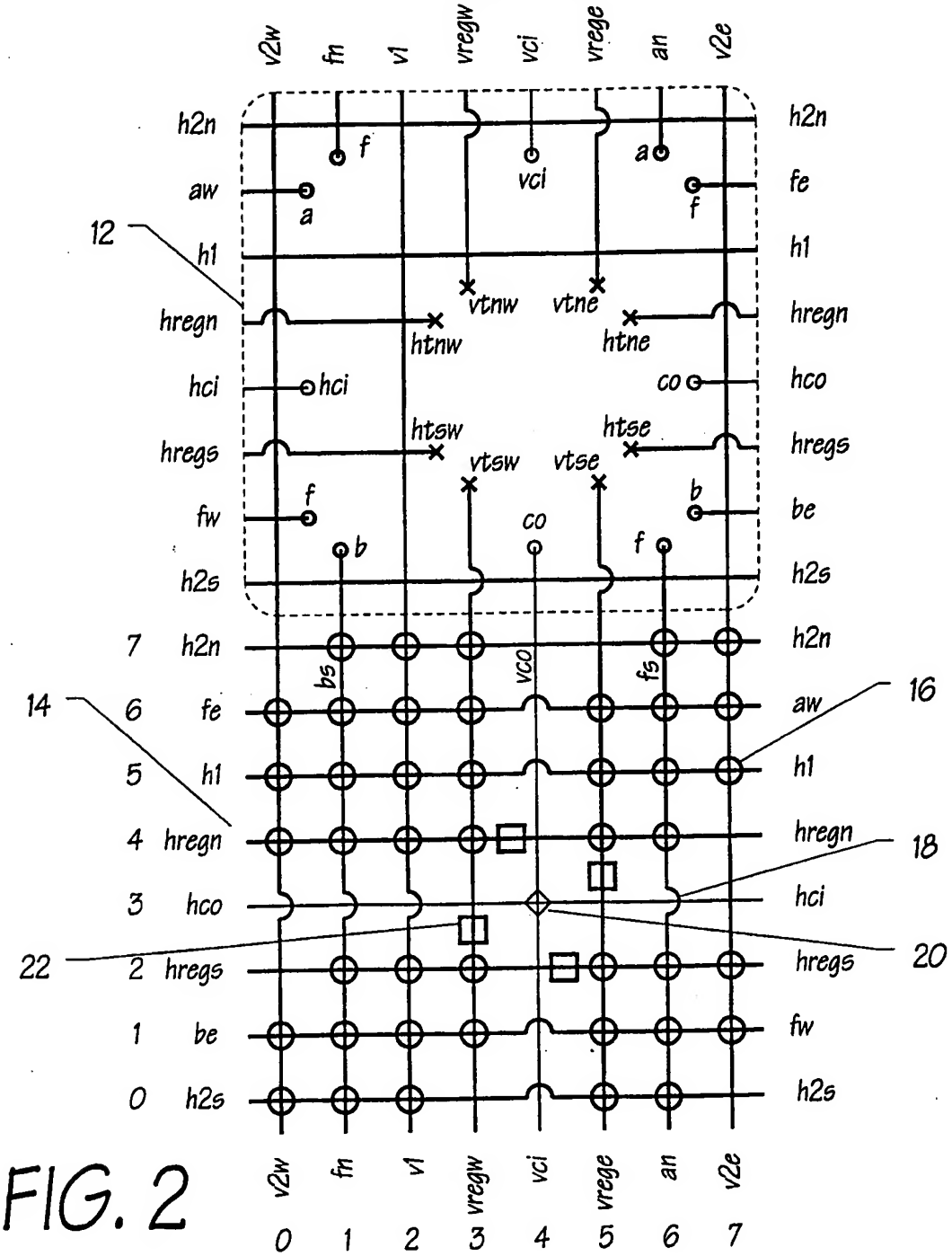


FIG. 2

= x-x selectably connectable to y-y (Figure 6A)

= x1 selectably connectable to x2 (Figure 6B)

= input to or output from ALU

= hco, vco selectably connectable to hci, vci or vci, hci (Figure 6C)

= permanent connection to long busses (Figures 3 to 5)

= permanent connection to register/buffer (Figure 9)

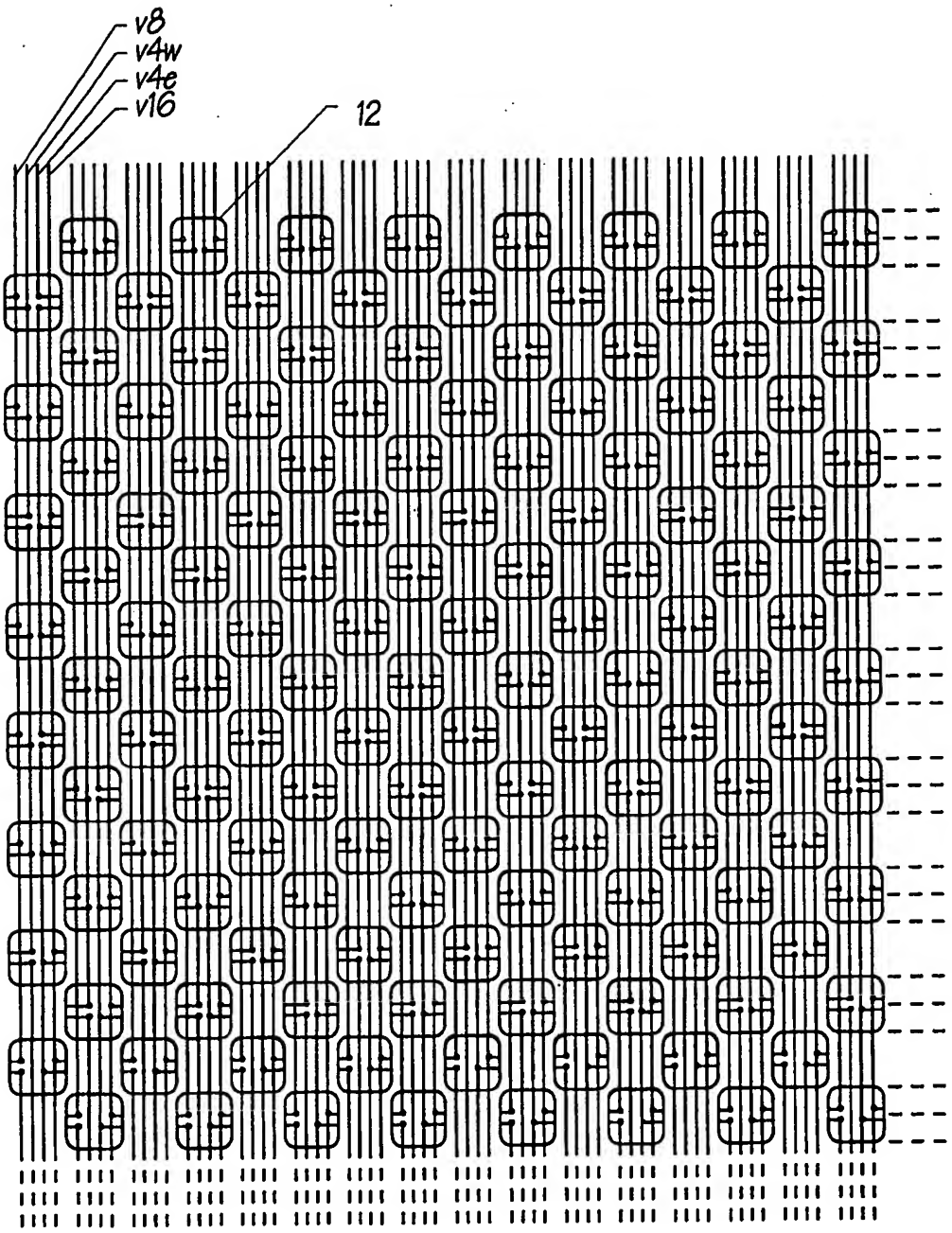


FIG. 3

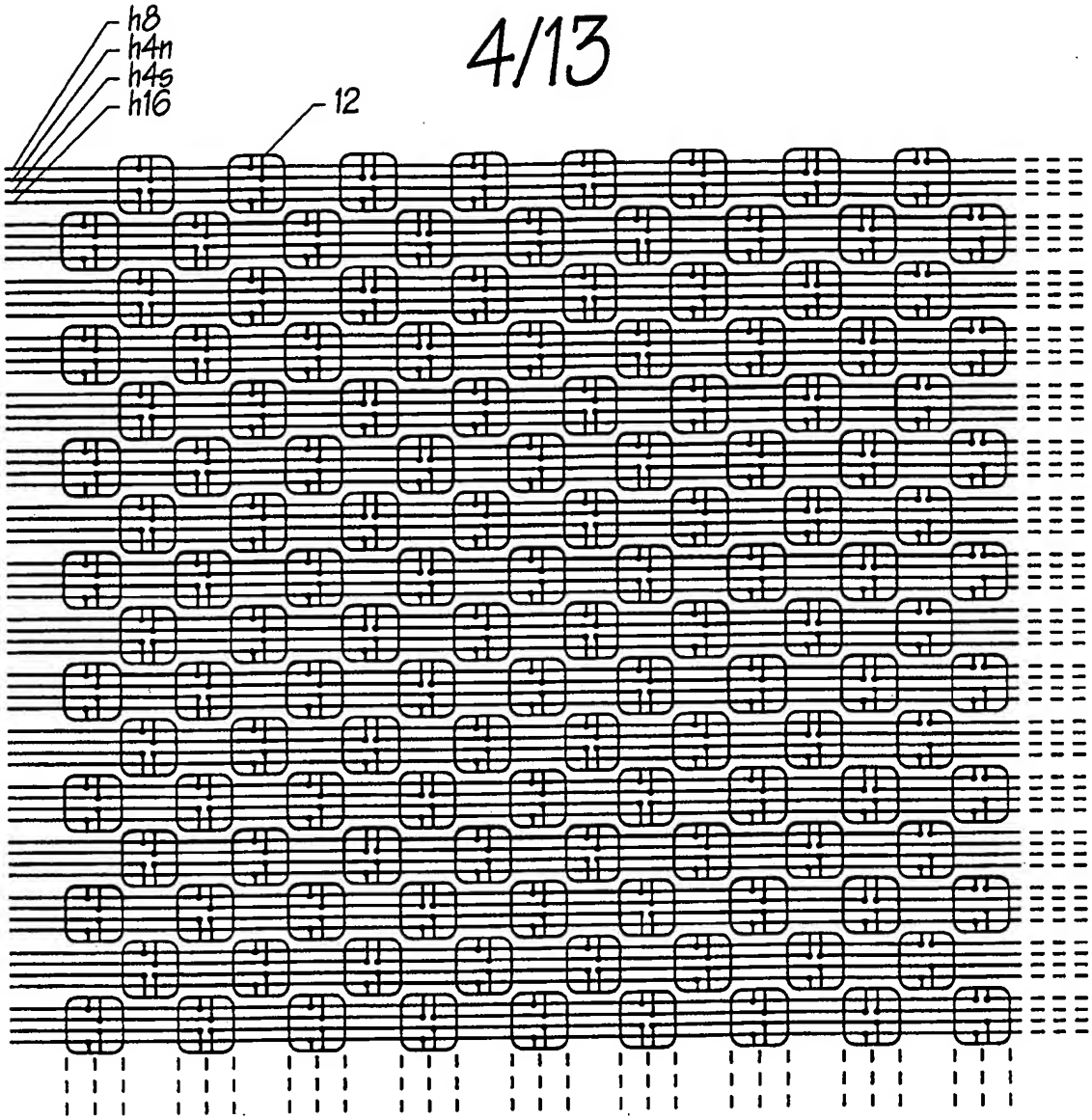

h8
h4n
h4s
h16
12

FIG. 4

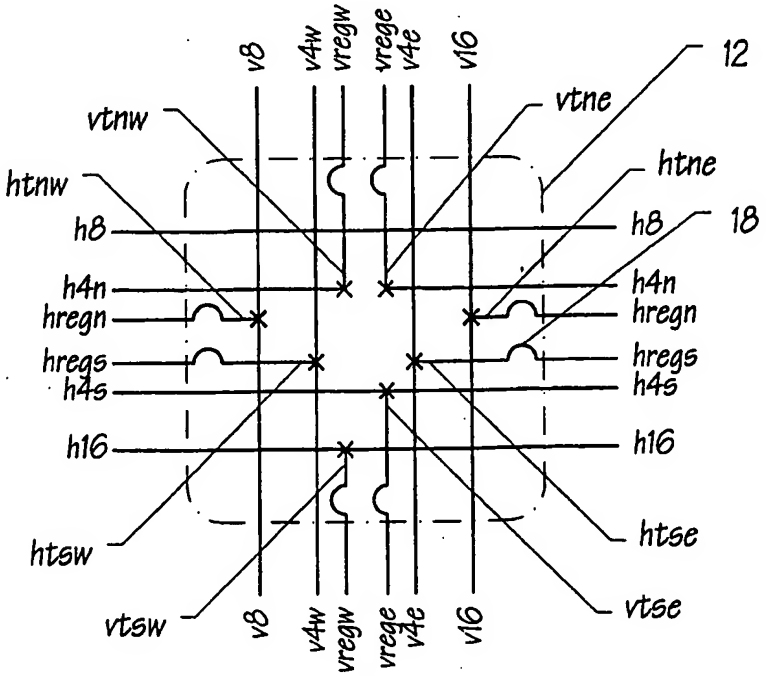

v8
v4w
vregw
vrege
v4e
v16
12
vtnw
vtne
htnw
htne
h8
h8
18
h4n
h4n
hregn
hregn
hregs
hregs
h4s
h4s
h16
h16
htsw
htse
vtsw
vtse
v8
v4w
vregw
vrege
v4e
v16

FIG. 5

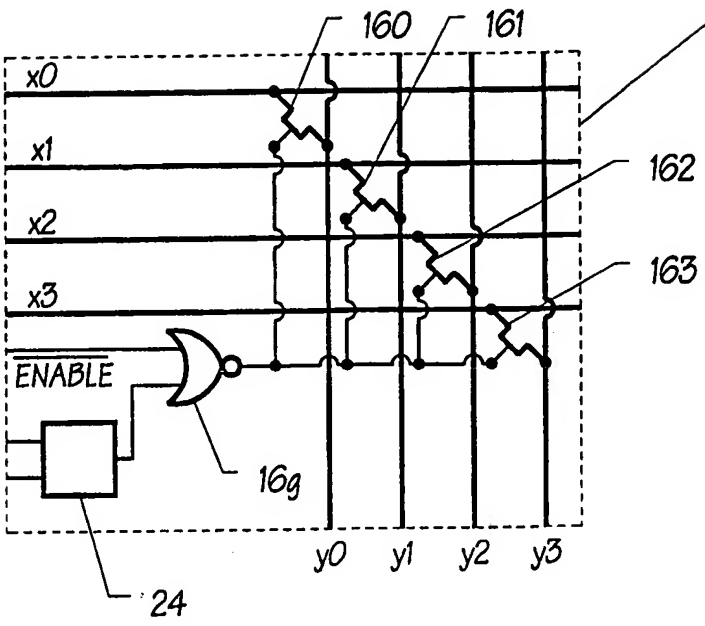


FIG. 6A

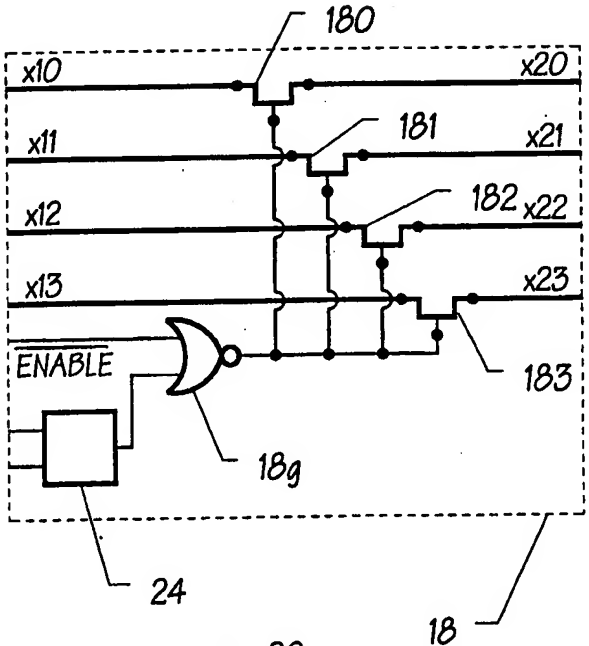


FIG. 6B

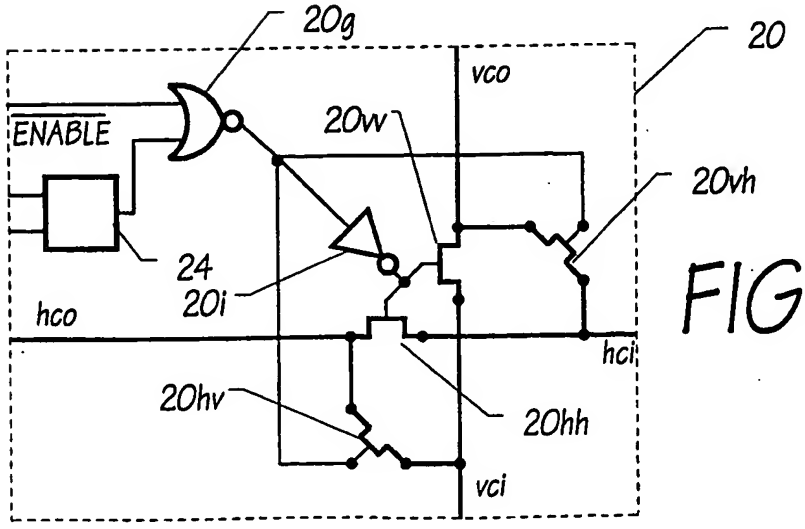


FIG. 6C

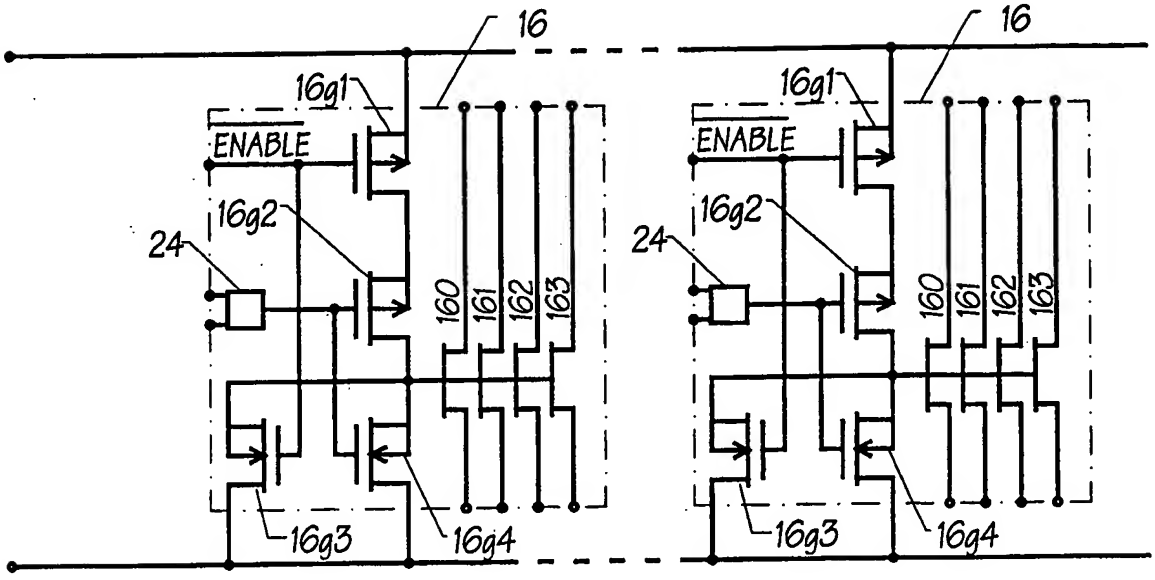

16
16g1
ENABLE
16g2
24
160
161
162
163
16g3
16g4
16
16g1
ENABLE
16g2
24
160
161
162
163
16g3
16g4

FIG. 7

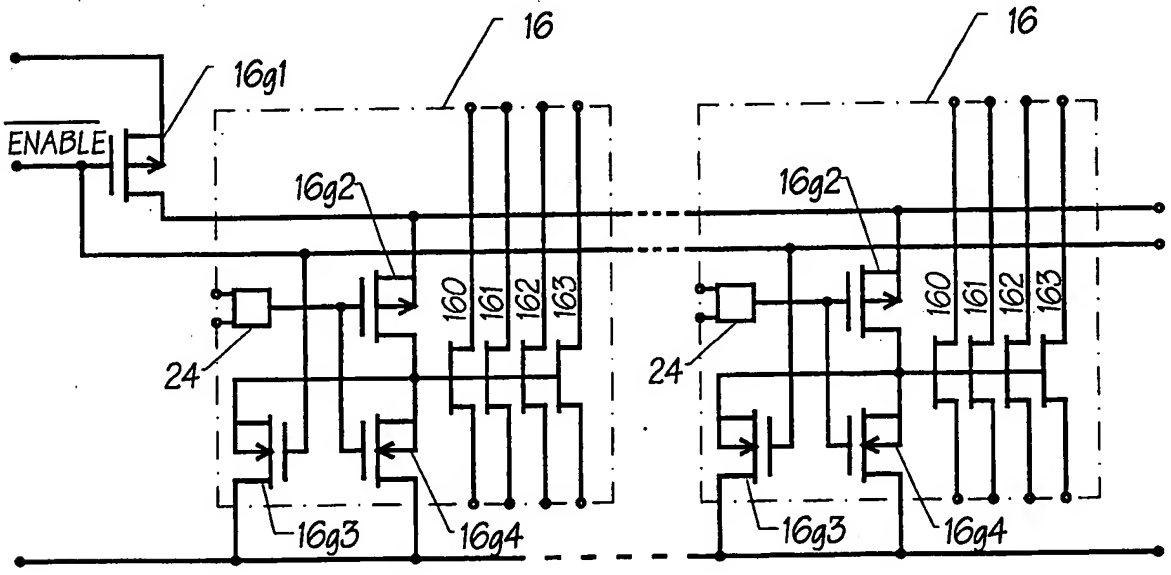

16
16g1
ENABLE
16g2
24
160
161
162
163
16g3
16g4
16
16g2
24
160
161
162
163
16g3
16g4

FIG. 8

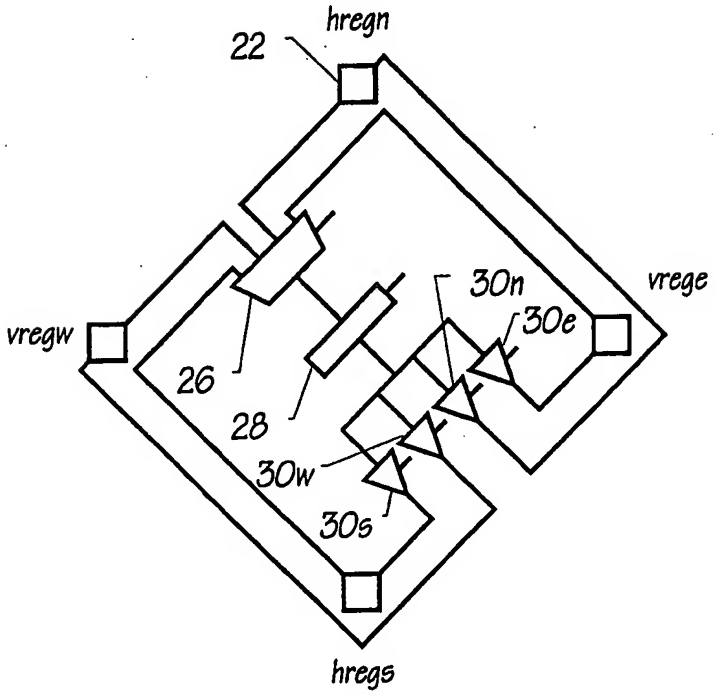

hregn
22
vregw
vrege
30n
30e
26
28
30w
30s
hregs

FIG. 9

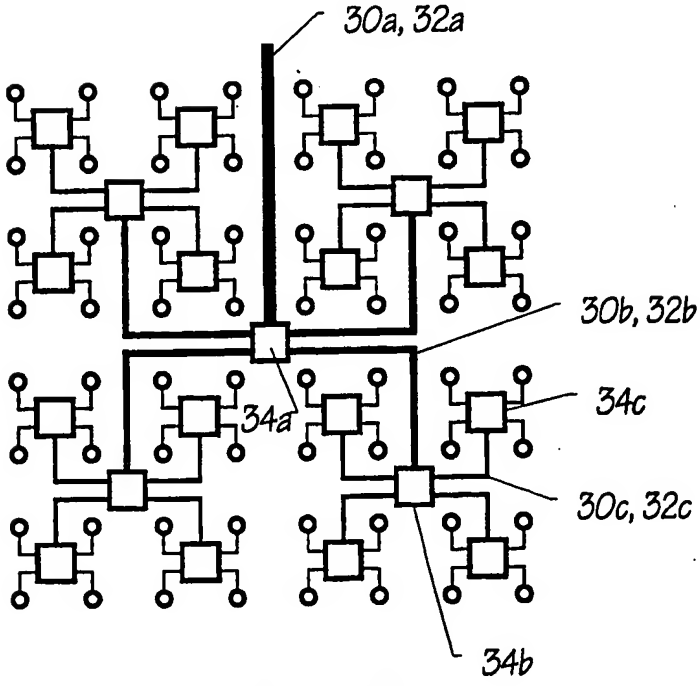

30a, 32a
30b, 32b
34a
34c
30c, 32c
34b

FIG. 10

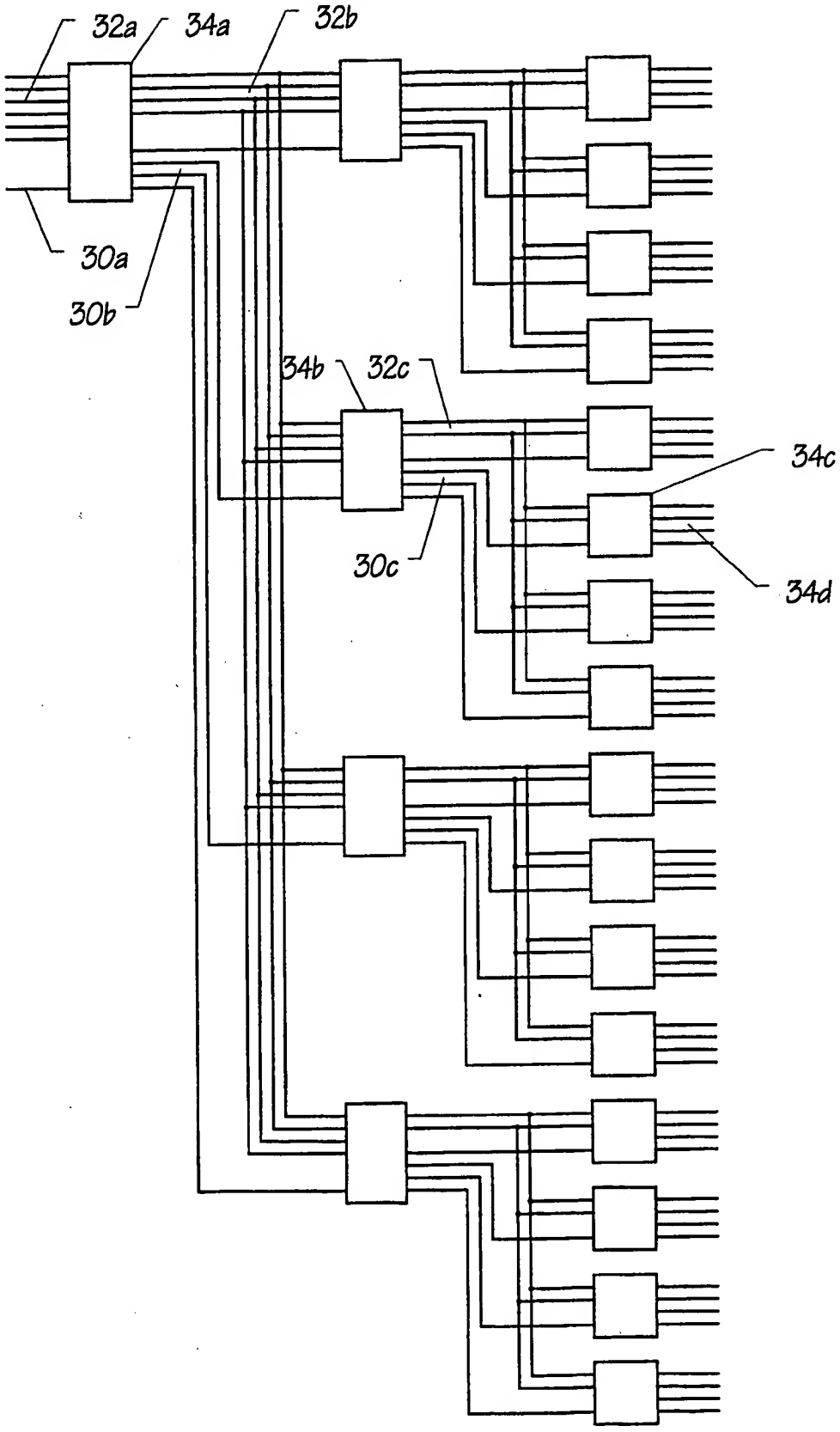


FIG. 11

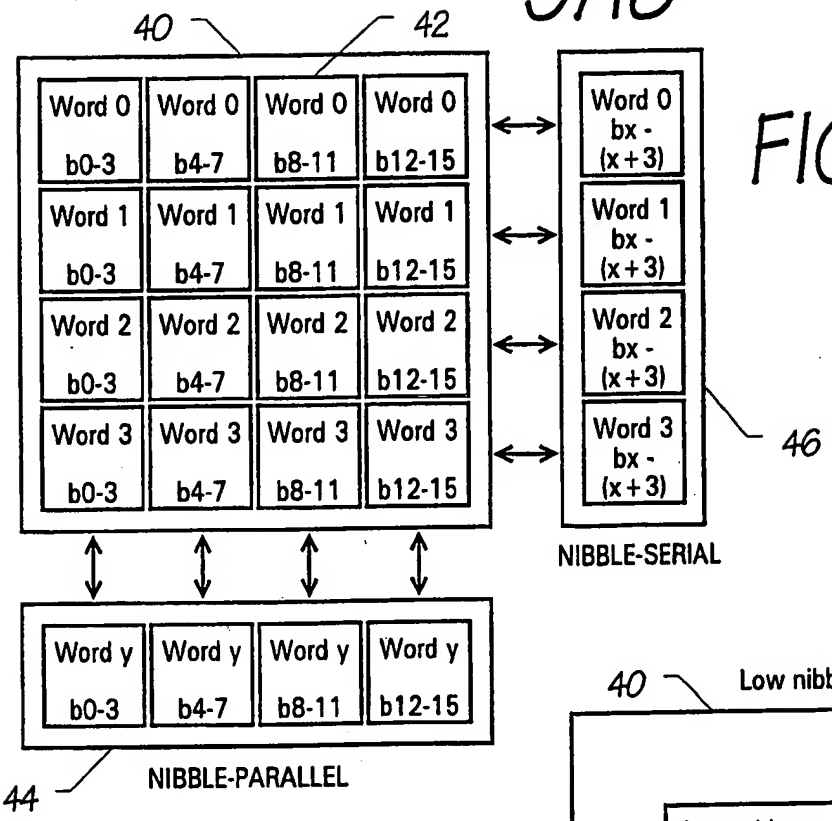


FIG. 12

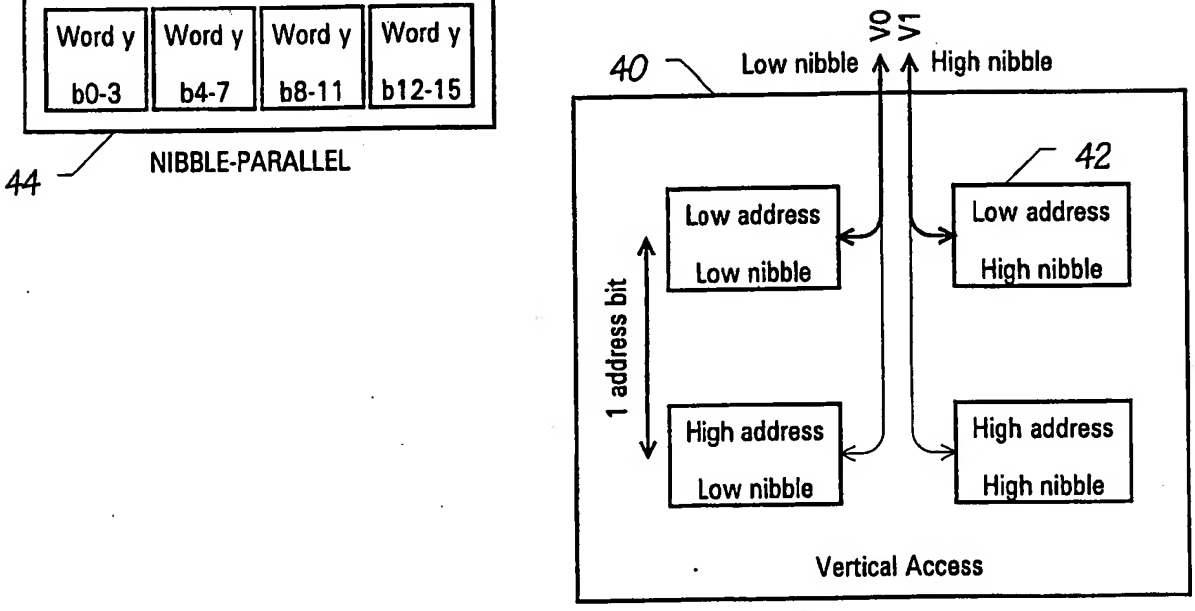


FIG. 13

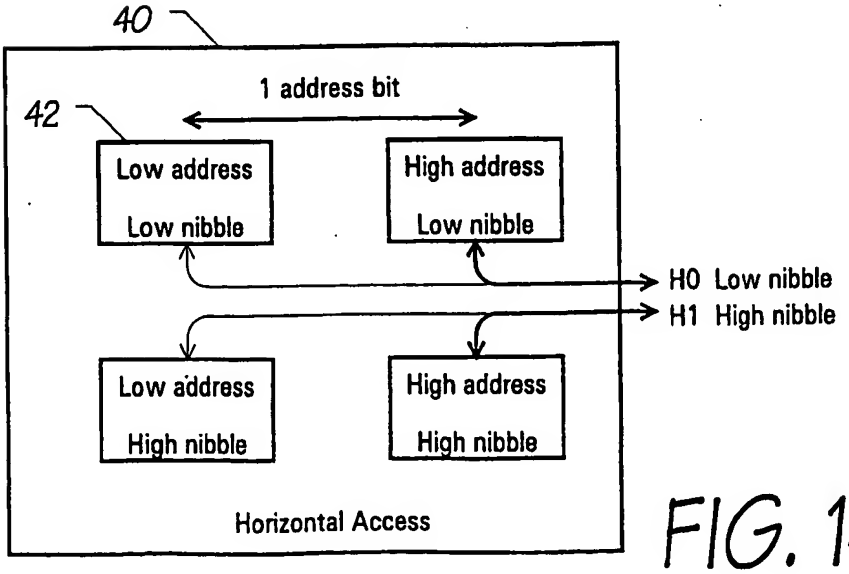
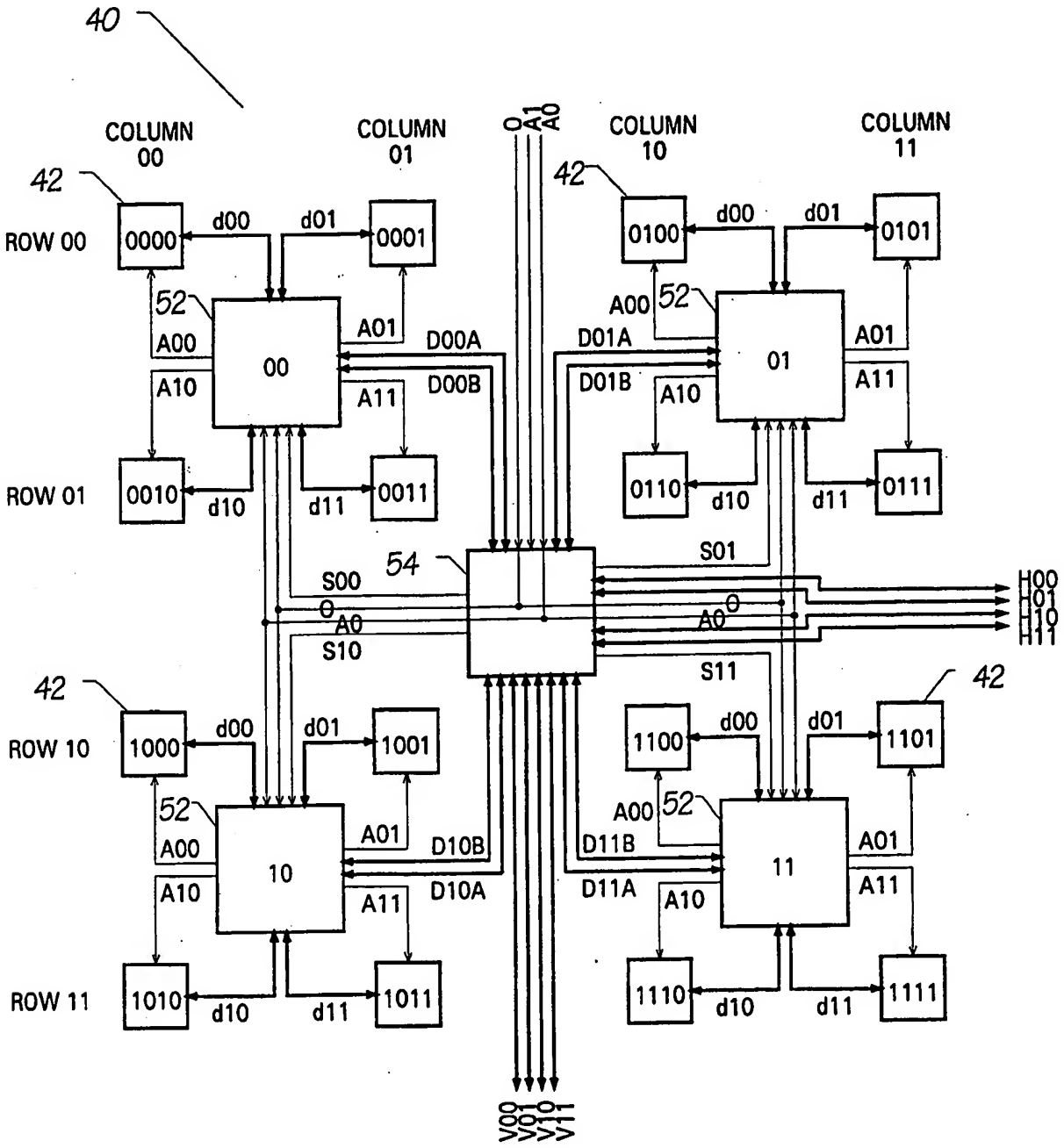


FIG. 14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V11

FIG. 15

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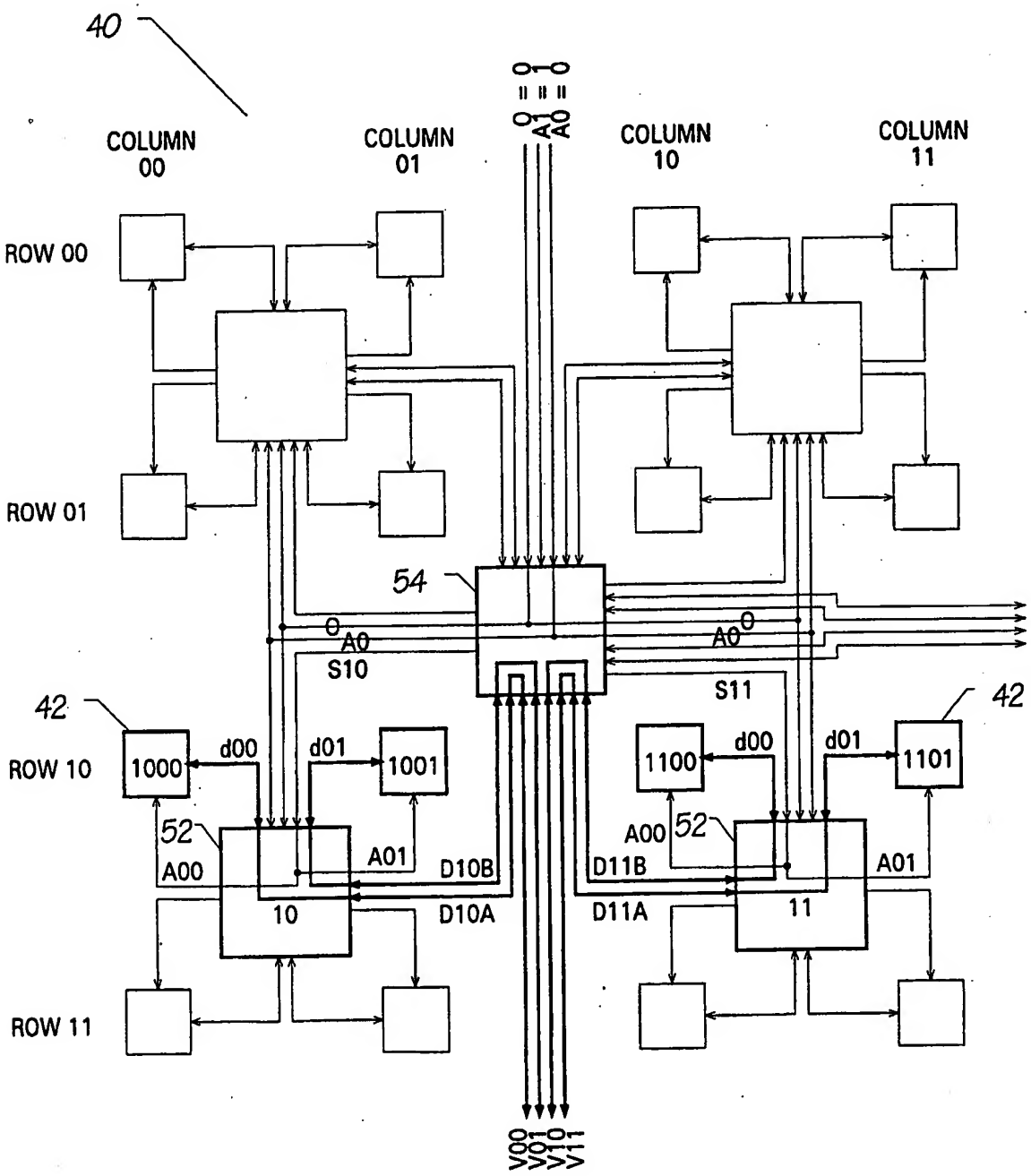
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FIG. 16

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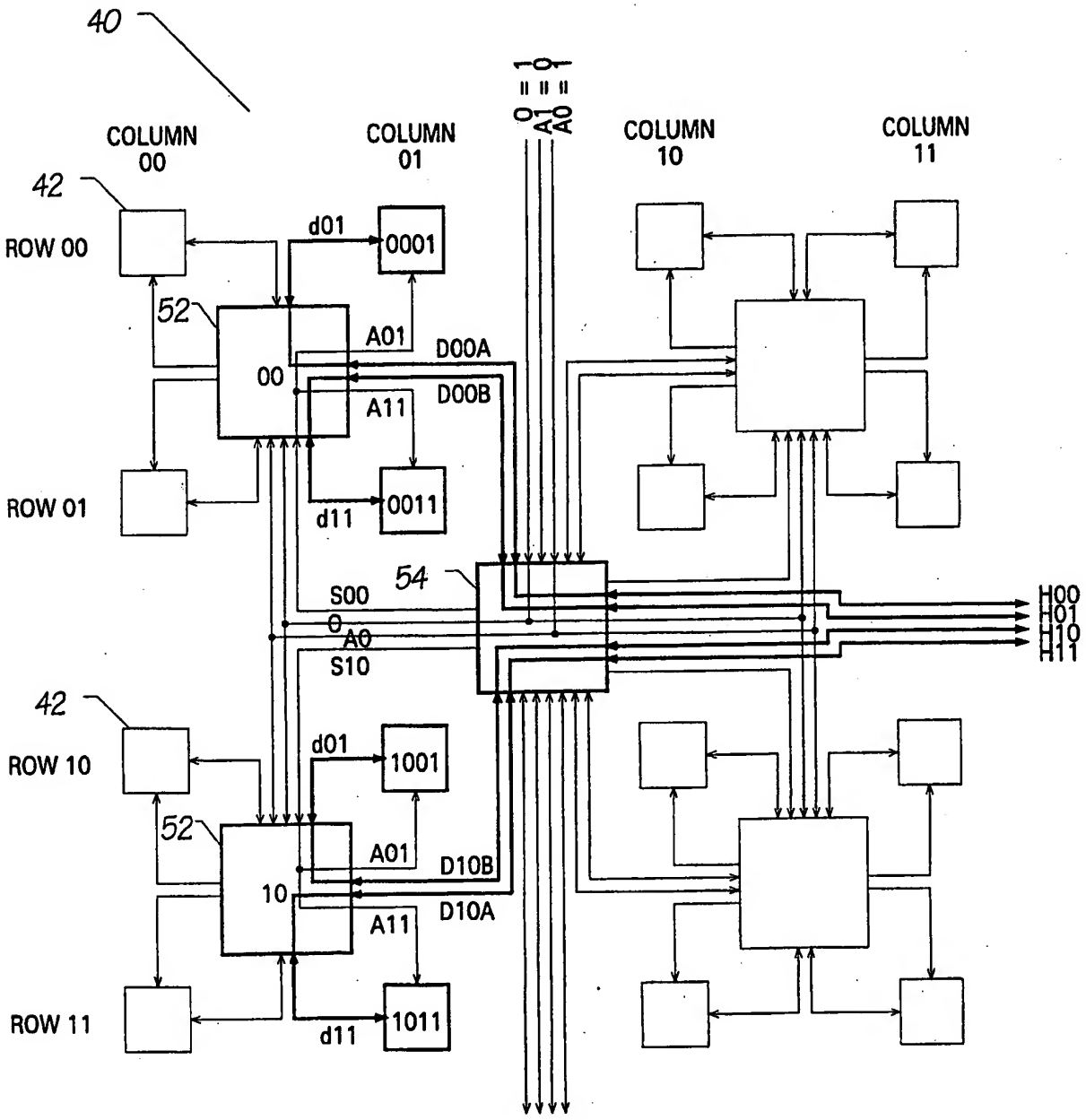
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FIG. 17

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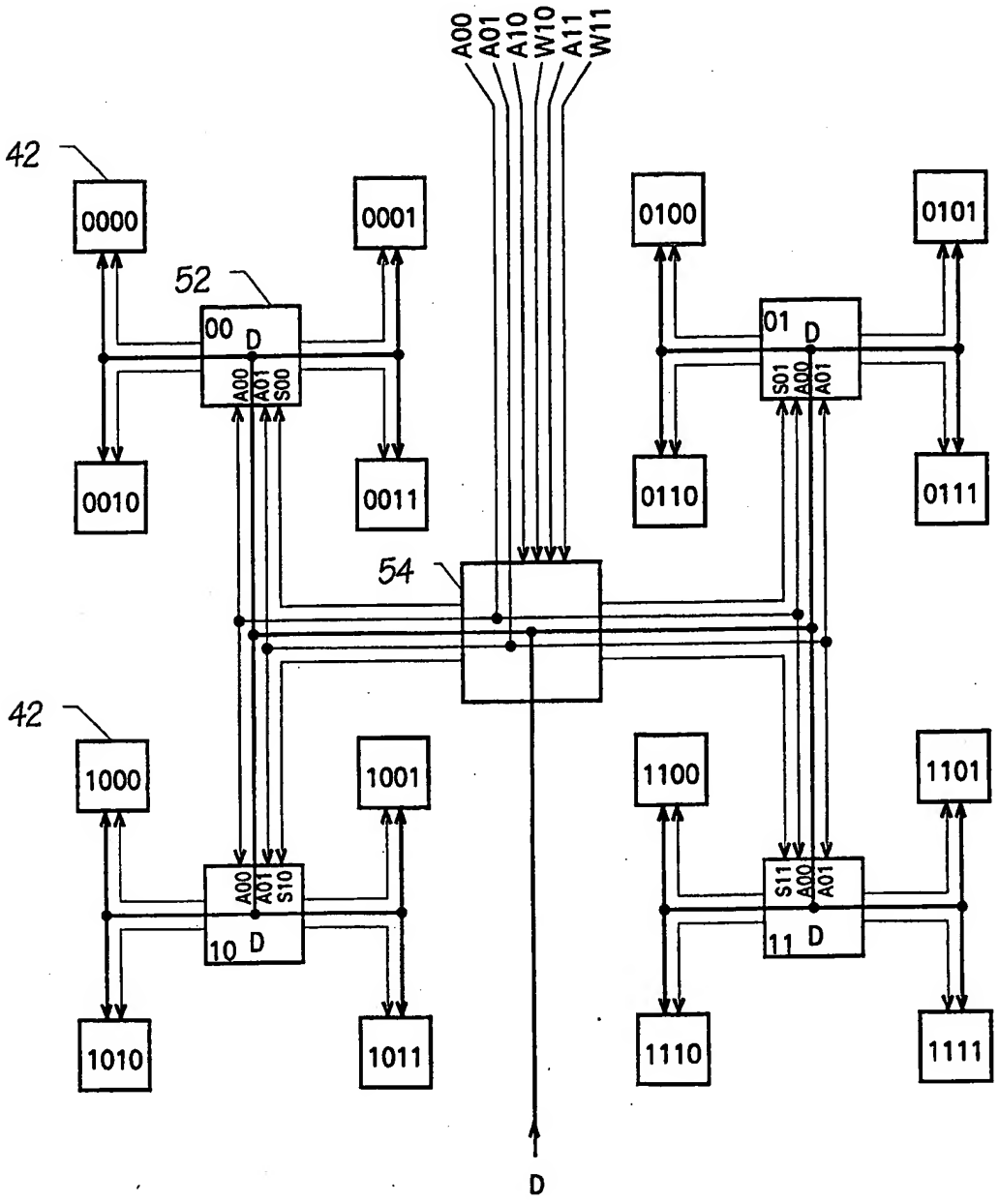
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FIG. 18

INTERNATIONAL SEARCH REPORT

Interi nal Application No
PCT/GB 98/00274

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G11C8/00 H03K19/177

According to International Patent Classification(IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G11C H03K

Documentation searched other than minimumdocumentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 972 380 A (HIDAKA HIDETO ET AL) 20 November 1990 see column 4, line 40 - column 5, line 14 see column 5, line 44 - column 6, line 56 see column 7, line 37 - line 42 see column 8, line 10 - line 56 see claim 3; figures 5,6	1-14
A	MAXFIELD C: "Logic that mutates while-u-wait" EDN (EUR. ED.) (USA), EDN (EUROPEAN EDITION), 7 NOV. 1996, CAHNERS PUBLISHING, USA, vol. 41, no. 23, ISSN 0012-7515, pages 137-140, 142, XP002064224 see page 138, right-hand column, line 3 - page 139, left-hand column, line 21; figures 3,4	6,7

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

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"&" document member of the same patent family

Date of the actual completion of theinternational search	Date of mailing of the international search report
11 May 1998	26/05/1998

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040. Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Michel, T

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Interr ıal Application No
PCT/GB 98/00274

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category ⁻	Citation of document. with indication.where appropriate. of the relevant passages	Relevant to claim No.
A	EP 0 667 681 A (TOKYO SHIBAURA ELECTRIC CO) 16 August 1995 see the whole document -----	8,9

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		JP 63312656 A	21-12-88
		US 5103426 A	07-04-92
EP 0667681 A	16-08-95	JP 7226082 A	22-08-95
		US 5680127 A	21-10-97